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**INFORMATION DISCLOSURE STATEMENT
BY APPLICANT**



Applicant: Florin UDREA

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Examiner: Pham, Hoai V.

Group Art Unit: 2814

U.S. PATENT DOCUMENTS

Examiner's Initials*	Document Number	Date MM/YYYY	Name (Family Name of First Inventor)	Class	Sub Class	Filing Date (if appropriate)
HP	AR	2002/0096708 A1	07/2002	Ahlers et al.		
	BR					
	CR					
	DR					
	ER					
	FR					
	GR					
	HR					
	IR					
	JR					

FOREIGN PATENT DOCUMENTS

		Document Number	Date MM/YYYY	Country	Inventor Name		Abstract		Readily Available	
							Enclosed	No	Enclose	No
HP	KR	1 026 750 A1	08/2000	EUROPE	Udrea					
HP	LR	WO 00/35023	06/2000	PCT	LetaVic					
HP	MR	2 380 056	03/2003	GREAT BRITAIN	Amaratunga et al.					
	NR									
	OR									
	PR									
	QR									
	RR									

OTHER (including in this order: Author, Title, Periodical Name, Date, Pertinent Pages, etc.)

HP	SR	Ng, R., et al., "Lateral Unbalanced Super Junction (USJ)/3D-RESURF for High Breakdown Voltage on SOI," 4 June 2001, pgs. 395-398.			
	TR	Udrea, F., et al., "Lateral Insulated Gate Bipolar Transistor (LIGBT) Structure Based on Partial Isolation SOI Technology," 8 May 1997, pgs. 907-909.			
	UR	Chen, X.B., et al., "Lateral High-Voltage Devices Using an Optimized Variational Lateral Doping," Int. J. Electronics, 1996, Vol. 80, No. 3, pgs. 449-459.			
HP	VR	Amberetu, M., et al., "150-V Class Superjunction Power LDMOS Transistor Switch on SOI, 4 June 2002, pgs. 101-104.			
	WR				
	XR				
	YR				

Examiner

Waylawn

Date Considered:

12/30/04

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.